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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,162	01/11/2002	Shahram Mostafazadeh	NSC1P225R	3102

22434 7590 09/07/2005

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,162	MOSTAFAZADEH ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/16/2005 has been entered.

Reissue Applications

2. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,117,710 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

3. The reissue oath/declaration filed with this application is defective (see 37 CFR 1.175 and MPEP § 1414) because of the following:

The originally filed reissue application stated the reason of being "partly inoperative" in US Patent No. 6,117,710 by the limitation of the leads extend "radially from a central opening" in claim 1 so that this limitation was deleted from the claim. The amendment to claim 1 now adds this limitation "radially from a central opening" back to the claim. Therefore, the error stated in the declaration is not adequate to meet the requirement of specifying an error that supports the reissue within the meaning 37 CFR 1.175(a)(1) and MPEP 1414, because the stated error "radially from a central opening" is not being corrected by the claims currently pending.

4. Claims 1-6 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175. The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

Response to Amendment

Affidavit

5. The affidavit filed on 05/02/2005 under 37 CFR 1.131 has been re-considered but is ineffective to overcome the Melton et al. reference.

6. The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Melton et al. reference to either a constructive reduction to practice or an actual reduction to practice. Specifically, the affidavit establishes conception prior to March 26, 1996. However, the affidavit fails to provide evidence that diligence exists from the date of conception to the date of constructive reduction to practice, the effective date of the instant reissue application. Accordingly,

the affidavit is inadequate to disqualify the Melton et al. US patent No. 5,844,315 as prior art against the applicant.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Djennas et al. US 5,474,958 in combination with Ogawa et al. US 5,252,855 and Pace US 5,904,499.

The Djennas et al. reference discloses methods for making semiconductor device having no die supporting surface. Throughout the description of the embodiments, the Djennas et al. reference discloses "there may be other embodiments of the present invention which are not specially illustrated", col. 2, lines 65-67, the "placement and geometry of the leads on the lead frame and of the conductive traces on the substrate are not restricted by the present invention", col. 12, lines 1-3;

Re claims 1 and 7, in the first embodiment, figs. 4-6, the Djennas et al. reference discloses a method for making semiconductor device having no die supporting surface comprising:

forming a flat lead frame including a plurality of leads extending radially from a central opening, "no tie bars, such as shown in FIG. 1 of the prior art", col. 4, lines 10-11, the lead frame *inherently* having opposing upper and lower surface;

the lead frame and an integrated circuit die are mounted onto a supporting work holder, "the stiffness of the wire bond 26 is sufficient to hold the semiconductor die 22 in

place during handling, transport, and most importantly, the molding process", col. 4, lines 37-40;

forming a plastic casing over an upper surface of the die and the upper surface of the lead frame;

the die *inherently* includes a plurality of die bond pads so that "the active surface of the semiconductor die 22 is wire bonded to the plurality of conductors 12", col. 4, lines 20-22 (*re claims 2-3)*.

In the alternative embodiment, the third embodiment of figs. 9-10, "the inactive surface of the wire bonded semiconductor die 22 is placed directly on a lower mold platen 92 includes a vacuum line 94 ... aids in the prevention of flash ... a heat sink (not illustrated) can be attached to the exposed inactive surface of the die 22 for enhanced thermal dissipation. In addition to the aforementioned advantages of device 58, another advantage to device 90 is that the total thickness of the device has been decreased because the package body 96 is not a total encapsulation of the semiconductor die 22. It should be obvious that although device 90 is illustrated to be a J-lead type of device, other external leads configurations are possible", col. 6, lines 19-50.

The two embodiment do not use removable tape to provide a temporary die supporting surface but used the mold platen or supporting work holder.

In the sixth embodiment, figs. 18-20, a "removable tape 148 is affixed to the bottom surface of the substrate 100 including the die cavity 102 ... the tape 148 provides a temporary die supporting surface whereupon the semiconductor die 22 is placed", col. 9, lines 6-12;

the step of forming the plastic casing comprises molding plastic onto the upper surfaces of the die and the substrate, fig. 19 (*re claim 6)*;

"the removal of the tape 148 from the bottom of the substrate 100 after the step of molding", col. 9, lines 49-51, whereby exposed portions of the substrate form the only externally accessible I/O contacts for the package, fig. 20.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the lead frame of the first embodiment, modified by the third embodiment to expose the lower surface of the die, with the removable tape of the sixth embodiment as suggested by Djennas et al. because the removable tape would provide support during handling, transport, and most importantly, the molding process (col. 9, lines 6-12), no vacuum needed for the wire bonding process (col. 9, lines 28-29) and to prevent flash during the molding process (col. 9, lines 39-41). Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sixth embodiment with the typical lead frame of the first and third embodiments without a die supporting surface because the lead frame without supporting surface would be selected in accordance with the method of forming flat device to prevent cracking at such locations 30, 32 and 34 as taught by Djennas et al. (col. 1, line 58 – col. 2, line 15, col. 5, lines 13-15).

The combination of the first/third embodiment with the sixth embodiment (in addition to the suggestions "placement and geometry of the leads on the lead frame and of the conductive traces on the substrate are not restricted by the present invention", col. 12, lines 1-3, and "other external leads configurations are possible", col. 6, line 49)

would provide the plastic casing comes into contact with the adhesive tape so that the lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die and exposed portions of the lead frame form the only externally accessible I/O contacts for the package and plastic fills at least portions of gaps between adjacent leads after removing the adhesive tape from the plastic casing.

The Djennas et al. reference discloses substantially all of the instant invention and ignores how the conventional lead frame is formed.

The Ogawa et al. reference discloses a method, figs. 1 and 3, using a lead frame without attached bumps wherein "a lead frame for use in a semiconductor package is made by punching with a pressing machine or by etching of a plate material", col. 1, lines 13-15 (*re claims 4-5*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Djennas et al. with the lead frame of Ogawa et al. because the lead frame of Ogawa would provide the package of Djennas et al. with improved reliability (Ogawa's col. 1, line 10). The method of forming the lead frame is well known in the art as taught by Ogawa.

With this combination, the exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package, these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board.

Further, the Djennas reference teaches "the external portion of the leads can be in any surface mount or through hole configuration... a heat sink may be attached to the inactive surface of the semiconductor die in any of the embodiments provided that the inactive surface is at least partially exposed... other methods of attaching the device to a board besides solder balls are anticipated as being suitable in practicing the invention" (col. 12). Furthermore, the Pace reference claims that its method is better than "conventional 'cavity up' packages where the heat has to be removed through the substrate into a printed circuit board", col. 6, line 64 to col. 7, line 3. It means that the mounting the package on a circuit board such that it is in directed contact with a heat sink formed on the circuit board is well known to those skills in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the board that has a heat sink so that when the package was mounted on the circuit board its die's lower surface would contact the 'heat sink' as a mean to conduct heat out of the package. The use of heat sink (the substrate) in the "cavity up" packaging process is well known to those skilled in the art as taught by Pace.

9. Claims 1-7 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melton et al. US 5,844,315 in combination with Ogawa et al. US 5,252,855 and applicant's admitted prior art.

Re claims 1 and 7, the Melton et al. reference discloses a method comprises the steps of: forming a flat lead frame 22 including a plurality of leads 13, the lead frame

inherently having opposing upper and lower surfaces; mounting the lead frame and an integrated circuit die 12 onto a molding support 38 of flexible polyimide tape having an adhesive coating such that a lower surface of the die contacts the adhesive tape and the die is located in a central opening, and the lower surface of the lead frame also contacts the adhesive tape, col. 2, lines 55-60; forming a plastic casting 21 *using a dispensing approach* over an upper surface of the die and the upper surface of the lead frame; and removing the adhesive tape 38 to expose the lower surfaces of the die and the lead frame, col. 4, lines 66-67.

Re claim 2, the die includes a plurality of die bond pads 36, and the method further comprises the step of electrically connecting each of the die bond pads to a selected one of the plurality of leads 13, col. 2.

Re claim 3, the step of electrically connecting comprises wire bonding, line 60 to col. 3, line 8.

Re claims 4 and 5, the forming the lead frame step comprises etching or stamping a metal sheet, col. 2, lines 43-45.

In the method of Melton et al., the lead frame provides the areas for plurality of bumps 20 to be attached, therefore after removing the adhesive tape the bonding surfaces 30 of the bumps are also exposed.

The Ogawa et al. reference discloses a method, figs. 1 and 3, using a lead frame without attached bumps and, *re claim 9,* "the joining surfaces of the metal members are provided with an anodic oxide film of copper or copper alloy" (col. 2, lines 58-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Melton et al. with the lead frame of Ogawa et al. because the lead frame of Ogawa would provide the package of Melton et al. with improved reliability (Ogawa's col. 1, line 10). With this combination, the "exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package", these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board, *re claim 10*.

Re claim 6, the combination does not disclose the formation of the plastic cap using a molding process.

Applicant admits this process of use molding approach to form the plastic cap is known in the art in the instant specification's col. 4, line 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the combination of Melton/Ogawa with the molding plastic on the upper surface of the die and the lead frame as taught by applicant's admitted prior art, because the molding plastic of applicant's admitted prior art would provide the method of the combination with a complete package.

The combination would provide the plastic casing comes into contact with the adhesive tape so that the lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die and exposed portions of the lead frame form the only externally accessible I/O contacts for the package and plastic fills at

least portions of gaps between adjacent leads after removing the adhesive tape from the plastic casing.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Melton et al./Ogawa et al. and applicant's admitted prior art as applied to claims 1-7 and 9-10 above, and further in view of Pace US 5,904,499.

Re claim 8, the combination does not teach mounting the package on a circuit board such that the lower surface of the die is in directed contact with a heat sink formed on the circuit board.

The Pace reference claims that its method is better than "conventional 'cavity up' packages where the heat has to be removed through the substrate into a printed circuit board", col. 6, line 64 to col. 7, line 3. It means that the mounting the package on a circuit board such that it is in directed contact with a heat sink formed on the circuit board is well known to those skills in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the board that has a heat sink so that when the package was mounted on the circuit board its die's lower surface would contact the 'heat sink' as a mean to conduct heat out of the package. The use of heat sink (the substrate) in the "cavity up" packaging process is well known to those skilled in the art as taught by Pace.

Response to Arguments

11. Applicant's arguments with respect to amended claims 1 and 7 (and their dependent claims) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

08/23/2005

George Fourson
Primary Examiner